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SYNTHESIS OF ASYNCHRONOUS DIGITAL SYSTEMS

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Abstract *: In present paper, the authors proposed a method for synthesis of the asynchronous digital systems using locally clock, [1]. In the design of the system are used different types of logic components as D type latches, logic gates. The entire system works fully asynchronous, means that it has no clock signal..*
Keywords *: Digital logic, FSM, Locally Clock, Fluence Graph, D Latch, Transition Table.*

1. INTRODUCTION

Driving an asynchronous digital system is a such complex task instead synchronous systems. In this paper, the authors propose an improoved method for the analisys and synthesis of an asynchronous digital system. For controll the transitions states of the digital system, it is build a locall signal named locally clock signal. Instead method presented in [1], the proposed method presented in this paper has many features like:

- execution speed much better;
- maximalize the combinational/sequential digital logic
- maximalize the design and implementation of the locally clock signal- CK, reset signal;
- maximalize the entire architecture means less logic design with improove funcionality.

A such of system is presented in figure 1. It contains the combinational logic modules, D type latches, input signals named input1,input2...inputN, output signals named output1,output2.....outputM, state variables named s1,s2...sk. The combinational system which implements the locally clock signal may be named synchronization module, it is used for controll the states of the digital system, disposal the hazard phenomenon from the digital systems. The entire system transit into a new state driving by the input signals which need to be stabile a period of time before changed and by the present states of the system.

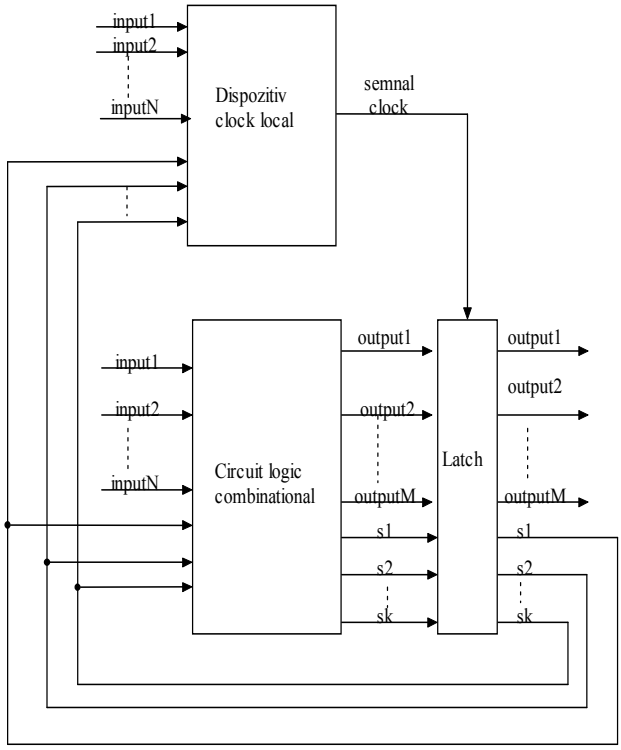

Figure 1

In figure 2 it's shown the consist modules of the digital system:

- locally clock generation device;
- combinational system who implements the system states equation ;
- D type latch1, latch2 are used to memorise the state of the system and also the outputs of the system;

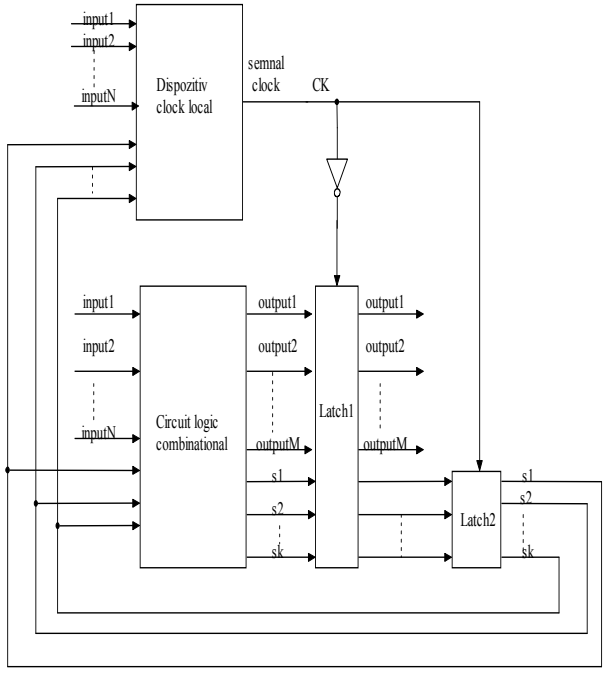

Figure 2

The locally clock signal (1) depends by the system's states notated with Q_i, input signals notated with X_j, where i=1,2,…n-1, j=1,2,…m-1; (n- states number variables, m-input number variables).

$$CK = F(Q_i, X_j) \quad (1)$$

If signal CK=1 the system will go onto a new state, if CK=0 the system will stay in present state, it will can read the output values signals. While the states and outpus signals are computed, the input signals will not be changed, the system will work in fundamental mode.

2. DESIGN AND IMPLEMENT A DIGITAL SYSTEM WITH LOCALLY CLOCK METHOD

Let's consider the fluence graph description of a digital system, figure 3.

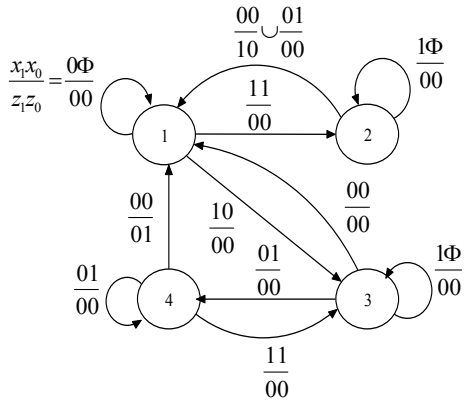

Figure 3

The fluence table is described in figure 4.

Q_{n+1}/z_1z_0

Q_n \ $(x_1x_0)_n$	00	01	11	10
1	1/00	1/00	2/00	3/00
2	1/10	1/00	2/00	2/00
3	1/00	4/00	3/00	3/00
4	1/01	4/00	3/00	-/--

Figure 4

The system's equations are described in (2):

$$\begin{aligned} D_1 &= y_{1,n+1} = [y_1(x_0 + x_1) + \overline{y_0}x_1\overline{x_0}]_n \\ D_0 &= y_{0,n+1} = x_{1,n} \\ z_{1,n} &= (\overline{y_1}y_0\overline{x_1}\overline{x_0})_n \\ z_{0,n} &= (y_1\overline{y_0}x_0)_n \end{aligned} \qquad (2)$$

The table from figure 5 shows the CK values, CK=1 if system transits onto a new state, different than present state, CK=0 if system remains in present state (next state equal with present state).

y_1y_0 \ $(x_1x_0)_n$	00	01	11	10
00	0	0	1	1
01	1	1	0	0
11	1	1	0	0
10	1	0	1	-

Figure 5

Using the Veitch-Karnaugh method it will compute the CK's equation (3):

$$CK = \overline{x_1} y_0 + x_1 \overline{y_0} + \overline{x_0} y_1 \overline{y_0} \quad (3)$$

Every output signal has attached an D type latch, the latch1 circuits memories the output values of the digital system, the D type latch2 memories the system's states variables.
After the CK signal become 1 logic (CK=1), the latch2 circuits are activated which memories the states of the system, after the time Φ (who depends by the delay through the combinational logic), the CK signal is automatically reseted (figure 6), the latch1 circuits will be activated and the values of the system's output are memorised. While the states and outpus signals are computed, the input signals will not be changed.

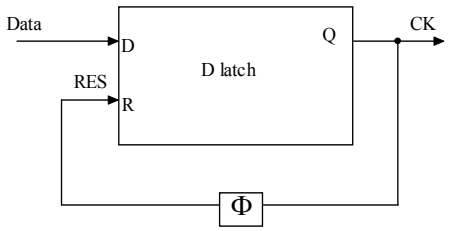

Figure 6

Functional diagram is related in figure 7.

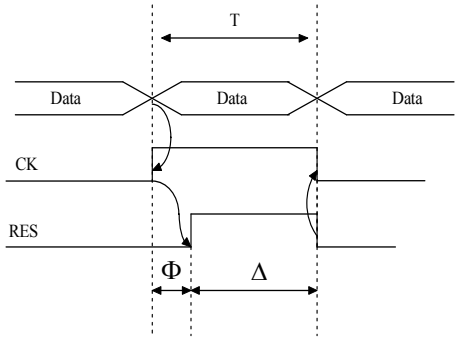

Figure 7

Φ - signals propagation time (delay) through the logic design, after that, the RES signal will be automatically activated.

Δ - the timing width of the reset command, during this period, the input signals x_1x_0 must keep the same values (not changed).

The (4) equations describe the rules need to be performed for correct functionality of the system:

$$\begin{aligned} &\Phi << T \\ &\Phi + \Delta = T \\ &\Delta \le T \\ &\Delta > \Phi \end{aligned} \quad (4)$$

The schematics design for the proposed digital system is shown in figure 8.

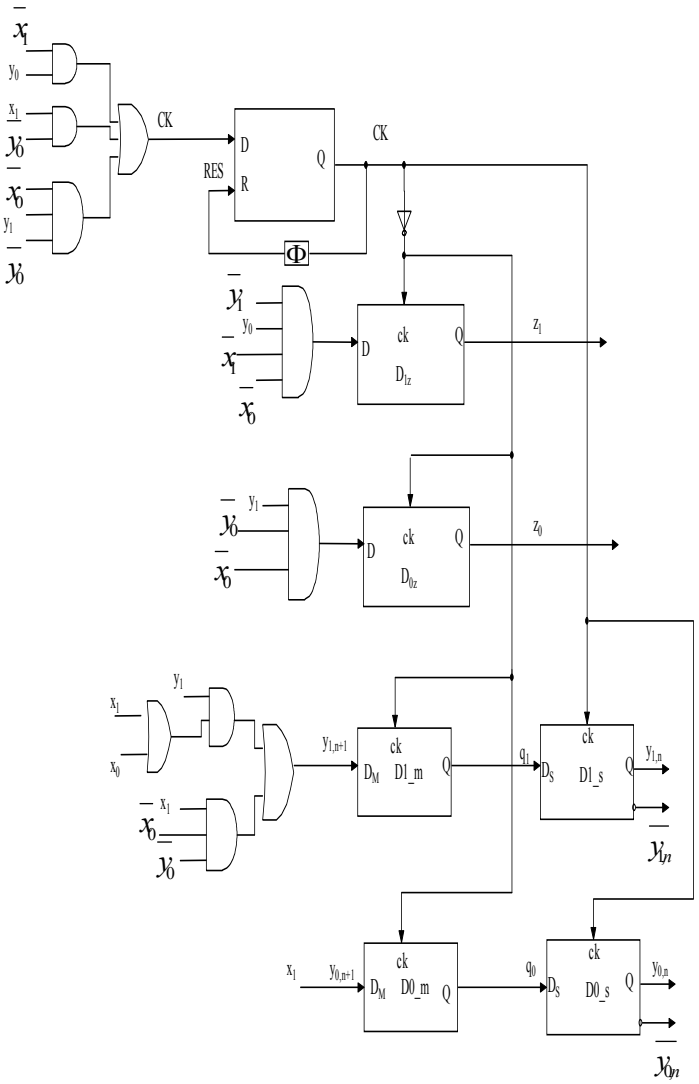

Figure 8

After timing compute for the entire system, results the (5) equation:

$\Phi = 313.6ns$ (5)

Performing this values, the entire digital system will work well.

Comparative with the classical locally clock method, this new method perform the reset command using the system from figure 6, the propagation timing delay through the system's logic modules. In this way, the system works faster and the possibilty of logic hazard are eliminated.

If the delay from Q signal to the Res signal has value $\Phi = 314ns$, the entire asynchronous system will work correctlly. For calculation of this delay can be used a RC circuit, equation (6), figure 9.

$$t(\mu s) = R(\Omega) \cdot C(\mu F)$$

$$R \cdot C = \Phi = 314ns$$

$$R = 20K\Omega \qquad (6)$$

$$C = \frac{R \cdot C}{R} = \frac{0.314\mu s}{20000\Omega} = 0.000015\mu F = 0.015nF$$

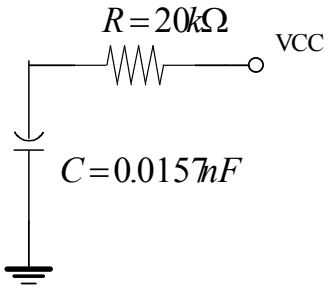

Figura 9

3. CONCLUSIONS

- The CK signal and the output signals must be free of logic hazard inorder to met the system run concordant with the specifications;
- The minimum propagation delay of CK signal through the combinational system must be greater than the maximum propagation delay for every logic circuit which implements the input/output signals.
- Once the CK signal is triggered it can be reseted without digital hazard.
- Usign the improoved design described above, the entire asynchronous digital system will work concordant with the specifications.

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